Siemens IT Solutions and Services PSE achieves first time silicon success using Analog Office design suite

Customer Background

Program and System Engineering PSE is a part of Siemens IT Solutions and Services, which pools the expertise of experienced IT services and solutions providers with that of renowned software development houses. Siemens IT Solutions and Services is represented in more than 40 countries and employs approximately 43,000 people. PSE's 7,000 high-tech experts at 22 locations in nine countries offer support to the Siemens Groups both as research and development partners and as system integrators and solution providers.

The Design Challenge

Siemens IT Solutions and Services PSE was faced with the challenge of designing several ultra-low-power, high-frequency receiver front-ends at 2.4 GHz, and 5.8 GHz for an embedded radio application. The team, which had previously used AWR's Microwave Office® design suite, and Visual System Simulator™
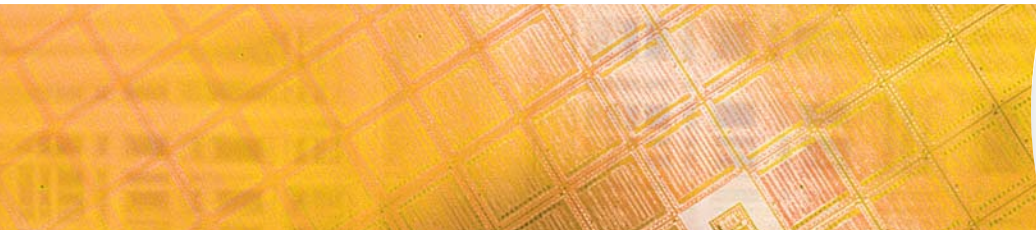
Customer:
Siemens IT Solutions and Services PSE

Application:
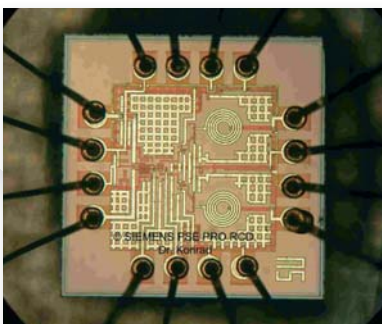High-frequency receiver front-ends at 2.4 GHz and 5.8 GHz

AWR Products:
Analog Office® design suite

product, needed a similar and efficient design approach for its RFIC work.

The requirements were extremely exacting: to deploy an intuitive, easy-to-use, RF-centric design environment that would support critical RF blocks with little

5.8 GHz RFIC front-end receiver

digital content. It was important to provide tight integration with the system simulation and electromagnetic (EM) tools, as well as robust frequency- and time-domain solvers, including productive layout and extraction capabilities. An open system was essential in order to integrate in-house physical verification tools. The software had to be capable of designing an RF chain from the antenna to the baseband, and from the system-level design down to layout in a single environment.

The preference was to use a PC-based design platform that would enable designers to easily interchange design files and use a flexible work schedule to support the existing RF system-centric workflow. In addition to design capabilities, it was necessary for the software to support silicon RF and silicon germanium (SiGe) foundry kits and to provide porting of foundry PDKs into the Analog Office environment.

"We wanted a design environment that allowed us to extend our RF engineering service offering to include RFIC design. Easy integration of the RFIC tool chain in our established, and proven product development workflow was very important for us, as RFIC design is a growing, but not the main activity in our daily business."

Dr. Wolfgang Konrad
Siemens AG Österreich
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The AWR Analog Office RFIC design environment was a perfect fit for what the Siemens team was looking for in an EDA tool suite. The first step was to port the existing foundry PDK into the AWR environment. The AWR support team worked jointly with the Siemens team to create and validate the electrical kit through automated wizards generating the symbols, schematics, and process models for the Analog Office tool.

The parameterized cells (PCells) were later derived by the Siemens team by interfacing the legacy, foundry-provided PCell generator, thus ensuring correct-by-design PCell compatibility.

The Analog Office software enabled the Siemens team to quickly complete their circuit simulations, both transient-domain using HSPICE and frequency-domain using AWR simulators. The tuning features enabled faster design of the critical circuit blocks, and different optimization algorithms were used in the Analog Office software to derive optimum performance with lowest noise.

The unique AWR unified data model, which supports electrical and physical co-design in one environment, enabled the Siemens team to interactively create the layout for the corresponding circuit. The unified data model enabled the Siemens team to perform RCLK parasitic extraction and simulation on a subset of the layout and routed blocks without having to wait for complete physical implementation.

The system- and circuit-driven design methodology provided an accurate representation of the layout and assured RF convergence, as the schematic and layout represented the same data and parasitic models. The final chip was validated for tape-out using the foundry-specified legacy sign-off tool, and experimentally using a Siemens internally-developed proprietary verification engine that was interfaced by the Siemens team to Analog Office through AWR's open design environment.

Because Analog Office software provides the same intuitive environment as the Microwave Office design style, the Siemens designers were productive from the start, cutting weeks of ramp-up time out of the overall design flow. Once the PDK porting efforts were finished, the AWR RFIC design flow in the Analog Office design suite enabled the Siemens team to tape out ahead of schedule, observe close correlation between measured and simulation results, and achieve first-time silicon success for the multiple chip design project.

"Since we were already using Microwave Office and VSS, we wanted the same easy-to-use, familiar environment for our RFIC work. We were pleased that the AWR RFIC design flow in the Analog Office design suite enabled us to tape out ahead of schedule, observe close correlation between measured and simulation results, and achieve first-time silicon success for our design projects."

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AWR is a member of Silicon Integration Initiative (Si2) and OpenAccess Coalition (OAC)

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